S3CP

OVERVIEW

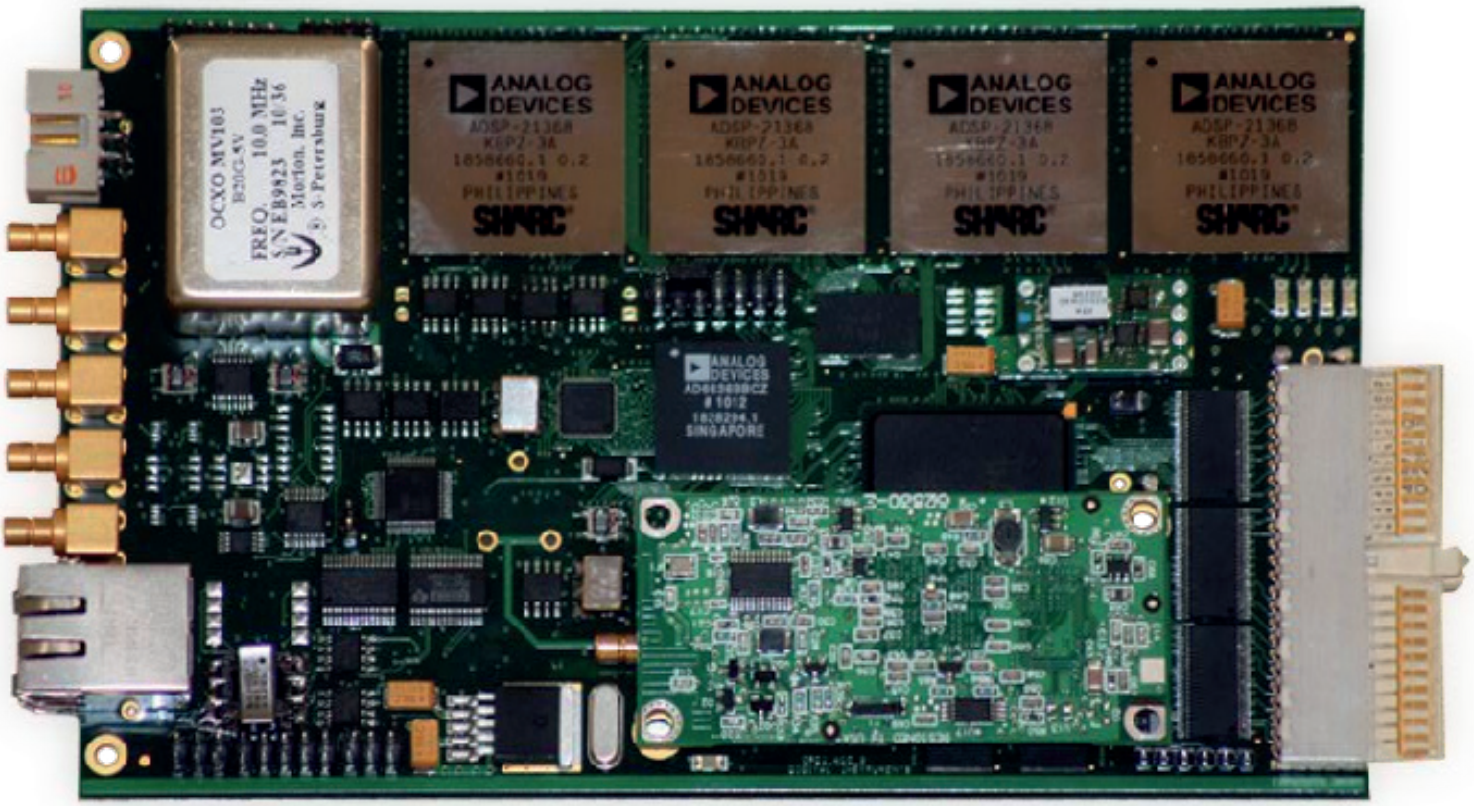
S3CP is a high performance real time processing card on a cPCI standard connector.

Mounted on S3CP there are **4 DSPs** working in a systolic cluster and a **FPGA** for hardwired processing and microprocessor activity. Conversion is made through IF Analog to Digital path, where the analog signal is sampled from AD at 150 MPs/s. BF analog signal is sampled too, using 2.5 MPs/s converter at 16 bit. RS signal is generated from DDS, where inside there is a 1 GHz NCO allowing the users to generate a wide spectrum of modulations, using I/Q datapath coming from FPGA/DSPs.

A wide range of applications are permitted. A FPGA microprocessor based is developed using **Microblaze™ XILINX** core, able to manage all the parts on the board.

A fully compliant cPCI bus standard allow the users to dialogue with more then one board over a cPCI backpane (Microprocessor unit is needed).

GPS receiver and a high stability OCXO guaranteed that all the processing write inside the FPGAs/DSPs are synchronous or time referenced via a built-in NTP server.
In the next hardware release the physical interface will be able to comply with the PTP protocol and enable the timestamping of real time events occuring in the host O.S. or triggered on the external SMB connectors.



Overview of the S3CP: in this picture the 4 DSPs are fully visible while the FPGA is partially covered by the GPS radio.

S3CP

HARDWARE

Parameters
· 1 IF input (SMB)
· 1 BF input (SMB)
· 1 PPS output (SMB)
· 1 10 MHz output (SMB)
· 1 RF output (SMB)
· 4 user signals outputs (TTL)
· 4 user leds
· 1 cPCI connector

IF Analog Processing
· A/D AD6640-150 MS/s 14bits,
· AD 6636 DDC, Digital Programmable VGA

BF Analog Processing
· A/D ADS1602, Digital Programmable VGA

RF Analog Processing
· D/A AD9957 DUC- 1Gs/s,
· Digital Programmable VGA

Digital Processing
· 1 Microblaze soft processor implemented on a Spartan-3ADSP 3400 running uClinux
· 4 x SHARCs processors Analog Devices
· ADSP-21368-DSP with 128 Mb x 32
· parallel RAM

SDRAM memory
· 1 GB DDR2 SDRAM
· 2 Independent 512 MB banks
· Max. bandwidth per bank: 2 GB/s
· Auto refresh capable
· Flash: 16 MB

Host & cPCI backplate interfaces
· cPCI - IP core included
· LEDs
· Micro JTAG header
· Additional cPCI backplate I/O possible

API
· API for 64-bit Linux
· Runtime FPGA programming, hardware control and application communication.

Application development software
· Support multiple design !ows including VHDL and Verilog
· Compatible with Xilinx ISE and all major synthesis design !ows access to micro JTAG heater via backplate for Chipscope and iMPACT

OCXO & GPS
· 10 MHz sine wave (possibly square wave) high stability single oven OCXO.
· GPS Receiver: 12 Channels L1 1575.42 MHz
· Tracking: correlation up to 12 satellites

PTP Section
· Protocol: IEEE 1588-2002 (PTPv1)- to be replaced by PTP 1588-2008 (PTPv2)
· Role: Grandmaster clock source (GPS) or slave
· Timestamping: Hardware
· Precision: < 1 us

NTP Section
· Protocol: NTP version 4
· Role: Grandmaster clock source (GPS)
· Timestamping: Software

Form factors
· Standard full-height, full-lenght cPCI
· Height: 101 mm
· Lenght:160 mm

Electrical
· On-card power derived from 3.3 V, 5 V and 12 V FPGA power dissipation is application dependent
· 6-pin GPU-style header for applications that need more power.

Environmental
· Cooling: Air convection
· Operation T: 0-50 Celsius
· Storage T: -20 - 80 Celsius
· Relative humidity: 45 to 95% (non condensing)

Quality
· Manifactured to IPC610- Cla 2 standard
· Designed and Supplied to ISO9001:2000 certification ROHS compliant.

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DIAGRAM OPERATION